REMARKS

Claims 1-17 remain pending in the application. Claims 1, 11 and 17 have been amended. Claims 2 and 12 have been cancelled.

Claims 1, 3-5, 10, 11, 15 and 17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lampaert et al. (U.S. Patent Application 2002/0188920) (Lampaert).

Applicants respectfully traverse the stated rejection for the following reasons:

Applicants submit that the rejection of the cited claims is unwarranted, since the Examiner does not take into consideration major differences between Lampaert's teaching and Applicants'.

Briefly, Lampaert teaches a design method of using a predictive MOSFET layout. Applicants teach performing a Layout versus Schematics Verification (LSV). Lampaert only mentions but does not teach how to perform the LVS check.

1. Referring to item A on page 5 of the Office Action, it states that Lampaert teaches identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors. The Examiner contends that the use of such model for design processes inherently includes the identification of the RF MOSFET circuit elements.

   Applicants submit that the use of "such model for design processes inherently includes the identification of the RF MOSFET circuit elements". Lampaert states very clearly that "a sub-circuit model is used as a predictor of electrical behavior of MOSFETs". This statement means using a predetermined sub-circuit model to predict a design's electrical behavior. It does not rely on the "identifying transistors in a sub-circuit way" as the necessary step to complete the "electrical behavior predicting" process. As depicted in Fig. 8, Lampaert does not mention

"identifying transistors" altogether. So, the "inherently" terminology is not sustainable.

Further, LVS is only **mentioned** in Lampaert's patent, e.g., in Fig. 8, element 810. Lampaert does not teach nor suggest **how to perform LVS**. By being moot on **how to perform LVS**, it implies that Lampaert is unable to address an essential aspect of the present invention, particularly, since it is well known that a traditional LVS method does not work for sub-circuit devices. Thus, Lampaert teaches away from Applicants' teaching on how to perform LSV.

2. Referring now to item 'B' in page 6 of the Office Action: "Lampaert teaches physical verification [fig. 8 element 810 – LVS, paragraph 0055...]". Again, the same argument applies here, namely, Lampaert only mentions LVS as it is taught by the prior art, but fails to teach how to perform it.

   As for a new design method dealing with "sub-circuit based device model", the traditional LVS method does not work, since Lampaert fails to teach how to perform it.

3. Regarding item C (page 6 of the Office Action) the same comments as those mentioned in item B also apply here.

4. Referring to item D, Applicants submit that paragraph 0056 describes "a layout generator generates a layout based on RF MOSFET parameters 'Wf', etc." It does not teach how to measure MOSFET parameters from the layout.

5. Referring to item E, again, no reference is made nor suggested how to implement LSV.

Accordingly, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Lampaert, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 11, 14-16 stand rejected under 35 U.S.C. 102(e) as being anticipated by Li (US Patent Application Publication 2004/0025125).

As a matter of record, Applicants are confused about the numbering used in the Office Action. By way of example, on page 4, the numbering 3, 4, 11, 15, 5, 6, 6, 7-9, 12-14 and 16 are confusing as to their meaning. Applicants fail to understand whether these numbers refer to identifiable paragraphs in the Office Action (in which case, these paragraphs should be numbered sequentially) or whether they refer to the claims. Clarification is earnestly solicited.

Notwithstanding the above, with regard to the above rejection of claims 11, 14-16 as anticipated by Li, Applicants traverse the above rejection for the following reasons:

On page 6 of the Office Action -- item F, the Examiner states that Li teaches providing device model parameters that support an extraction of a list of device layout geometric parameters [paragraph 0006-0008]; and provide specific marker shapes to define the layout geometric parameters.

Applicants submit that paragraphs 0006-0008 of Li does not teach "providing model parameters that support an extraction of a list of device layout geometric parameters", as stated by the Office Action. There are many geometric parameters associated with a sub-circuit based device of which Li is moot, e.g., providing marker shapes which are generated to mark errors, **which are required in order to perform the operations taught by the Applicants.** Applicants provide marker shapes as a design shape to identify a device. Accordingly, the respective teachings are different.

Referring to item I of the Office Action, Applicants contend that Li, in paragraph 0043, describes a "dummy" usage. It is solely used for density or manufactureable check, and it is not used for layout verification LVS purposes.

Regarding Claims, 3, 4, 5 and 10, Applicants submit that they all depend of Claim 1. Since Applicants believe that Lampaert does not teach the same invention as Applicants', then, neither does Lampaert teach those claims that are dependent on Claim 1.

On page 4, item 11, The Office action states that Li teaches ".... a method for creating a device layout comprising the steps of: ... geometric parameters [paragraph 0006, paragraph 0008]"

Applicants contend that Paragraph 0006 and 0008 describe the layout design process and layout extraction process. Applicants teach "providing device model parameters..." especially a sub-circuit based device model which supports a complex layout extraction with a list of sub-circuit geometric parameters. This key step is not taught nor suggested by Li., in addition to similar arguments already provided supra when addressing the rejection of claims 1 and 17 in view of Lampaert.

The Office Action further states that Li teaches "providing specific marker shapes to define the device layout geometric parameters ... [paragraph 0092]"

Applicants contend that the "marker geometries" in paragraph 0092 refers to a "DRC error marker geometries generated by an electronic design automation (EAD) tool..." It is used for erroneous edge segments in the DRC process. The marker shapes in claim 11 is a design layer/shape, and a component of a sub-circuit device layout needed for layout verification. Thus, the two markers referred by Li and the markers taught by Applicants are totally unrelated to each other. Applicants submit that if the markers referred by Li were utilized in the present application, such markers would have been totally useless to satisfy the execution of the remaining steps taught in the independent claim.

Regarding the rejection of Claim 14 (dependent on claim 11), the Office Action recites: "wherein said devices are selected from the group consisting of bipolar junction transistors (BJT), hetero-junction bipolar transistors (HBT), and compounded semiconductor transistors [paragraph 0008 – transistors, which includes BJT, HBT, and/or compounded semiconductor transistors]. Applicants contend that in addition to Claim 14 being dependent on claim 11, in Paragraph 0008 – transistors, which include BJT, HBT, and/or compounded semiconductor transistors is to cover common sense layout extraction for all other types of transistors.

Applicants submit that claim 14 teaches a sub-circuit based layout extraction and verification, which as explained earlier is not possible to achieve with markers taught by Li.

The Office Action further recites for claim 15, "wherein further marker shapes are added to non-FET devices ... [paragraph 0043]."

Applicants contend that Paragraph 0043 utilizes a marker layer to optimize the layout design, such as optimizing ground and power line wiring. The marker layer taught by the Applicants provides layout extraction and verification assistance.

The Office Action states that in claim 16, "non-FET devices are selected from the group consisting of integrated on-chip inductors ... [paragraph 0039].

Applicants submit that Paragraph 0039 teaches a non-orthogonal geometries treatment whereas Claim 16 teaches a sub-circuit based extraction and verification for the non-FET devices, such as resistor and capacitor, all of which are not taught nor suggested by Li.

Thus, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Li,, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Accordingly, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Li, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Notwithstanding the arguments submitted, in order to advance the prosecution of the present application, Applicants have opted to amend claims 1, 11 and 17 incorporating all the limitations the base claim and any intervening claims.

In view of the foregoing amendments and arguments, Applicants respectfully request that all the rejections and objections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,
RAMINDERPAL SINGH, ET AL.

By: /H. Daniel Schnurmann/
H. Daniel Schnurmann
Agent for the Applicants
Registration No. 35,791
Tel. (845) 894 2481